

# ADS7864MEVM

This user's guide describes the characteristics, operation, and use of the ADS7864MEVM 12-bit parallel analog-to-digital converter evaluation module. A complete circuit description, a schematic diagram, and bill of materials are included.

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## 1 EVM Overview

### 1.1 Features

- Full-featured evaluation board for the ADS7864 250-KHz, 16-bit, 6-channel simultaneous sampling analog-to-digital converter
- Analog inputs can be configured as single-ended or differential
- Modular EVM format allows connection to C5000™ and C6000™ DSK platforms through the 5-6K Interface Board.
- Built-in reference
- High-speed parallel interface

C5000, C6000, C2000, TMS470 are trademarks of Texas Instruments.

## 2 Introduction

The ADS7864 contains two high-speed 12-bit A/D converters that operate from independent +5-V  $V_{DD}$  and  $D_{VDD}$  supplies. Each A/D in the chip is preceded by a 3:1 multiplexer, providing six total input channels. The parallel digital output is provided as a 16-bit word which contains both channel address information and conversion data results.

Each of the six input channels contains a fully differential sample-and-hold circuit arranged into three pairs (A, B, and C). Each channel pair has a hold signal (HOLDA, HOLDB, and HOLDC) which, when strobed together, allows simultaneous sampling of all six analog inputs. The device accepts an analog input voltage in the range of  $-V_{REF}$  to  $+V_{REF}$ . The ADS7864 also accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry (see Figure 1).

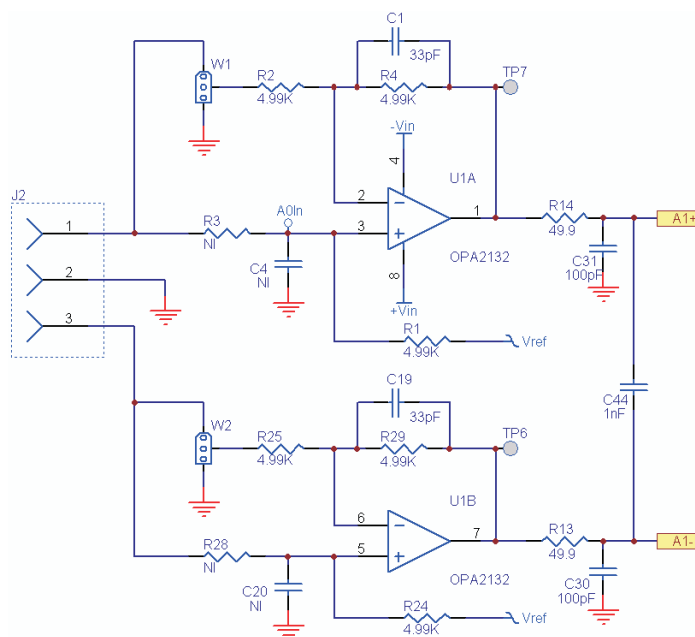
Conversion time for the ADS7864 is  $1.75 \mu s$  when an 8-MHz external clock is used. The corresponding acquisition time is  $0.25 \mu s$ . To achieve maximum output rate (500 kHz), the read function can be performed at the start of the next conversion cycle.

## 3 Analog Interface

The analog input to the ADS7864 is divided in two parts. Connector J4 provides access to input channels A1 and B1 through two different amplifier circuit configurations. The input buffer configuration of channel A1 presents a typical front-end circuit for the A/D converter. Its function is to provide level and impedance adaptation of the input signal. The input to channel B1 is a bipolar configuration using the INA159 to accommodate  $\pm 10$ -V input signals. Connector J3 provides access to the remaining analog input channels through a simple R/C filter.

### 3.1 Analog Input – Channel A1

The analog input to the ADS7864MEVM board for channel A1 is comprised of the dual OPA2132 operational amplifier and the associated circuitry as shown in Figure 1. The OPA2132 is powered from the  $\pm 12$ -V analog supply, and arranged as an inverting amplifier with a gain of 1. The internal  $+2.5$ -V reference voltage of the ADS7864 is applied to the noninverting input of the OPA2132 to provide input bias.



NOTE: Components marked NI are NOT INSTALLED.

Figure 1. ADS7864MEVM Schematic – CHA1 Input

This configuration allows single-ended signals of  $\pm 2.5\text{-V}$  ( $+5\text{-V}_{pp}$ ) to be applied to either the (+) or (-) input of channel A1 (via J2 pin 1 or 3 referenced to pin 2). The input also can be applied to connector J4 (not shown) pins 2 or 4, referred to analog ground.

### 3.2 Bipolar Input to Channel A1

By changing resistor components and setting the appropriate jumpers, it is possible to configure the input buffer to accept bipolar input voltages. Table 1 is related to the schematic presented in Figure 1 and represents just a few of the possible input configurations.

**Table 1. Typical Analog Input Buffer Circuit Values**

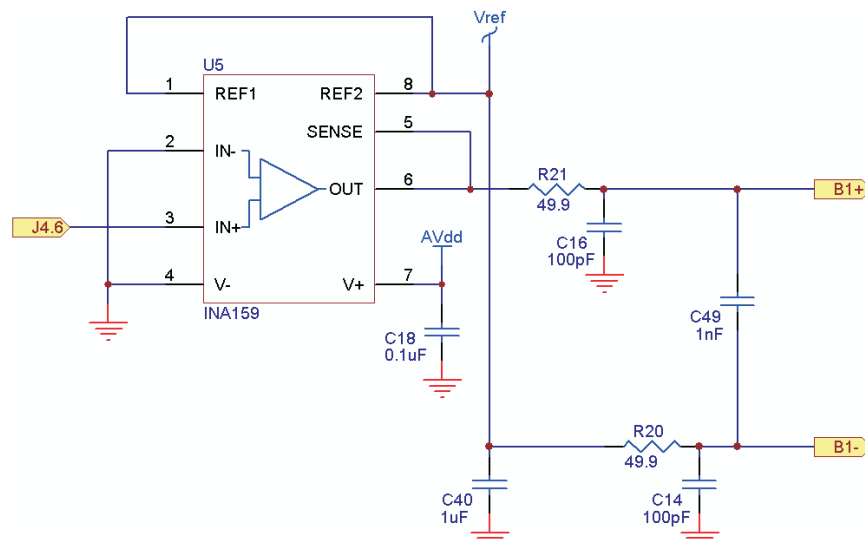
	Input Voltage	R3 R28	R2 R25	R1 R24	R4 R29	W2 W1
See Figure 1	Default 0 – +5	open	5 k $\Omega$	5 k $\Omega$	5 k $\Omega$	1–2
	0 – 2.5	5 k $\Omega$	5 k $\Omega$	open	5 k $\Omega$	2–3
	– 2.5 – +2.5	20 k $\Omega$	4 k $\Omega$	20 k $\Omega$	4 k $\Omega$	2–3
	– 5 – +5	20 k $\Omega$	4 k $\Omega$	10 k $\Omega$	2 k $\Omega$	2–3
	– 10 – +10	20 k $\Omega$	4 k $\Omega$	5 k $\Omega$	1 k $\Omega$	2–3

The output from the buffer stage in each case applies 0 V to 5 V to the CHA1(+) input when the applied signal is connected to J2 pin 1 or J4 pin 2. The applied signal is directed to the CHA1(-) input when connected via J2 pin 3 or J4 pin 4.

When operating the ADS7864 with single-ended signals it is important to keep the unused ADC input biased to +2.5 V. This is easily accomplished on the EVM by changing the components associated with either the inverting or noninverting only, leaving the default component values shown above on the unused input. For example, to achieve a bipolar input range of  $\pm 10\text{ V}$  on CHA1(+), use the component values shown above for R1–R4 and move the shunt on W2 from position 1-2 to position 2-3. Components R24, R25, R28, and R29 and the shunt on W1 should remain in the default conditions shown in Table 1

### 3.3 Analog Input – Channel B1

The analog input to the ADS7864MEVM board for channel B1 is comprised the INA159 difference amplifier and the associated circuitry as shown in Figure 2. The INA159 is powered from the +5-V analog supply, and arranged as a noninverting amplifier with a gain of 0.2. The internal +2.5-V reference voltage of the ADS7864 is applied to both REF1 and REF2 pins of the INA159 to provide a direct  $\pm 10\text{-V}$  interface with built-in level translation to the noninverting input of channel B1.



**Figure 2. Channel B1 Input Circuit**

### 3.4 Analog Inputs –Channels A0, B0, and C1/C0

The analog inputs to the remaining ADS7864 input channels are routed to connector J3 and configured with simple R/C filters only. This configuration allows the EVM user to apply any customized input circuit to the data converter. Connector J3 is comprised of a male/female pass-through combination of pin header and socket with industry standard 0.1-inch centers.

When the ADS7864MEVM is used in combination with the 5-6K Interface Board or HPA-MCU Interface board, the DAP Signal Conditioning Board ([SLAU105](#)) can be used to drive the remaining input channels.

## 4 Digital Interface

The ADS7864MEVM is designed for easy interfacing to multiple control platforms. Jumper options are provided on the EVM to allow control over the state of Chip Select pin ( $\overline{CS}$ ) as well as the operating mode pins (A0–A2) the Reset pin ( $\overline{RST}$ ) and the Conversion Start strobes (HOLDA, HOLDB, and HOLDC).

Jumpers W4 and W6 control the signals applied to A0, A1, A2 and  $\overline{CS}$ . In the factory default mode, W6 is closed by means of a shunt jumper. The Ax and  $\overline{CS}$  pins are controlled by the signals applied to J5 (top or bottom side). When used with either the 5-6K or HPA-MCU Interface Boards, these control signals are associated with the host processors address bus.

By removing the shunt jumper located at W6, the A0, A1, and A2 pins are controlled by shunt jumpers placed on W4. The  $\overline{CS}$  pin is routed to J5.1, which requires the application of an active-low Chip Select signal. A simple shunt jumper placed across J5 pins 1-2 can be used to force the  $\overline{CS}$  pin to ground if desired.

### 4.1 Parallel Control

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual-row header/socket combination at J5 ([Table 2](#)). This header/socket provides access to the digital control pins of the EVM. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for a variety of mating connector options.

**Table 2. Header/Socket Combination at J5**

Pin Number	Signal	Description
J5.1	DC_CSa	Daughter Card Chip Select – active-low signal used to access the EVM
J5.3	DC_AWE	Write Strobe – signal not used on the ADS7864MEVM
J5.5	DC_ARE	Read Strobe – active low signal used to access parallel data
J5.7	EVM_A0	EVM Address line 0 – used with U3 to control A0
J5.9	EVM_A1	EVM Address line 1 – used with U3 to control A1
J5.11	EVM_A2	EVM Address line 2 – used with U3 to control A2
J5.13	EVM_A3	EVM Address line 3 – used with U3 and U6 to control /CS
J5.15	EVM_A4	EVM Address line 4 – not used
J5.17	DC_TOUT	Timer Input – optional CLK input used with W8
J5.19	DC_INTa	Interrupt Output to Host Processor – connects to the ADC's EOC pin

## 4.2 Parallel Data

The ADS7864MEVM uses Samtec part numbers SSW-116-22-F-D-VS-K and TSM-116-01-T-DV-P provide a convenient 16-pin, dual-row, header/socket combination at J6. This header/socket combination provides access to the parallel data pins of the ADS7864. Data line D0 is connected to J6 pin 1. Data lines 1–15 are located on pins 3–31, respectively. Even pin numbers 2–32 are connected to digital ground

## 4.3 GPIO/Control Options

Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P also provide a 10-pin, dual-row header/socket combination at J1 to facilitate general-purpose input/output (GPIO) control options to the ADS7864. [Table 3](#) describes the functions and pinout of J1.

**Table 3. J1 Pinout and Functions**

Pin Number	Signal	Description
J1.1	NA	Unused on the ADS7864MEVM
J1.3	NA	Unused on the ADS7864MEVM
J1.5	HOLD_C#	Active low signal HOLDC used to start a conversion on ADC channel pair C
J1.7	HOLD_B#	Active low signal HOLDB used to start a conversion on ADC channel pair B
J1.9	HOLD_A#	Active low signal HOLDA used to start a conversion on ADC channel pair A
J1.11	RESET#	Active low signal RESET used to place the ADS7864's FIFO in reset state
J1.13	NA	Unused on the ADS7864MEVM
J1.15	NA	Unused on the ADS7864MEVM
J1.17	DC_TOUTa	Used in conjunction with W10 to allow host processor timer control of HOLDx
J1.19	NA	Unused on the ADS7864MEVM

## 5 Power Supplies

The ADS7864MEVM board requires +5 VDC for the both the analog and digital section of the ADC. The supply (+Va and +Vd) can range from +4.75 VDC to +5.25 VDC. Because the EVM is designed to work with the 5-6K and HPA-MCU Interface Boards, JP1 provides direct connection to the common power bus described in [SLAU104](#). [Table 4](#) shows the pinout of JP1:

**Table 4. JP1 Pinout**

Signal	Pin Number		Signal
+VA (positive input buffer supply)	1	2	-VA (negative input buffer supply)
+5VA (+Va to the ADS7864)	3	4	-5VA (Unused)
DGND	5	6	AGND
+1.8VD (Unused)	7	8	+VD1 (Unused)
+3.3VD (used with W5 for support circuitry)	9	10	+5VD (+Vd to the ADS7864)

Alternate power sources can be applied through various test points located on the EVM. See the schematic at the end of this document for details. Note – although filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source.

## 5.1 Reference Voltages

The ADS7864MEVM is configured to use its internal reference through jumper W3 (see schematic for details). If an external reference is desired, the shunt jumper on W3 should be moved to cover pins 1-2; the external reference source then can be applied to the test point labeled TP10 referenced to TP12. The internal +2.5-V reference is still connected to the input buffer U1 in this case to ensure proper mid-point biasing to channel A1.

## 6 EVM Operation

The analog input swing is 5 Vpp, centered on a +2.5-V internal or external reference. The installed device accepts bipolar input ranges when a level shift circuit is used in the analog front-end circuitry. See section 3.2 of this document or section 12 of *Op Amps for Everyone* ([SLOD006](#)) for information on various circuit configurations. Channel B1 is factory configured for bipolar operation and is ready to accept inputs in the range of  $\pm 10V$  (see section 3.3 of this document).

Once power is applied to the EVM, the analog input source can be connected directly to J3 or J4 (top or bottom side) or through optional amplifier and signal-conditioning modules using the 5-6K and HPA-MCU Interface Boards. The analog input level (at the ADC) should not exceed 5 Vpp. The analog input range is from  $\pm V_{ref}$  (typically 2.5 VDC) centered at +2.5 V.

The digital control signals can be applied directly to J1 and J5 (top or bottom side). The ADS7864MEVM also can be connected directly to the 5-6K Interface Board for use with a variety of C5000™ and C6000™ series DSP Starter Kits (DSK), or the HPA-MCU Interface Board for use with C2000™ Series DSPs or TMS470™ Series controllers. The Control and Data connectors are designed to allow pattern generators and/or logic analyzers to be connected to the EVM using standard ribbon-type cables on 0.1-inch centers.

The BYTE signal, which controls the output of the ADS7864 when used with 8-bit controllers, can be manipulated with jumper W7. By default, W7 is closed and the BYTE pin is held low, providing data in 16-bit format. Removing the shunt on jumper at W7 asserts BYTE high by means of pullup resistor R23.

The conversion clock can be applied to J7, a BNC connector with a 50- $\Omega$  terminator, or J5 as mentioned previously. Jumper W8 allows the EVM user to select the clock source. In normal operation (factory default) the shunt on jumper W8 is covering pins 2-3. To use a clock source applied to the BNC connector J7, move the shunt at jumper W8 to cover pins 1-2. In either mode, the clock source can be monitored at TP21.

### 6.1 Default Jumper Locations

[Table 5](#) provides a list of jumpers found on the EVM and their factory default conditions.

**Table 5. ADS7864MEVM Jumpers**

Jumper	Shunt Position	Jumper Description
W1	Pins 1-2	Controls CHA1(+) input source selection
W2	Pins 1-2	Controls CHA1(-) input source selection
W3	Pins 2-3	Controls reference source (default is internal)
W4	OPEN	3X2 Jumper to control A0, A1, A2
W5	Pins 1-2	Controls BVdd Selection, should remain on pins 1-2 for the ADS7864
W6	Closed	Controls application of A0, A1 and A2 signals as well as the chip select input. Used in conjunction with W4.
W7	Closed	Controls BYTE input, opening W7 forces BYTE high via R23
W8	Pins 2-3	Controls application of conversion clock source via J5 or J7
W9	NA	W9 pins 2-3 are wired short on the PWB
W10	TIMER	3x3 Jumper to control HOLDx signals – timer or GPIO options available

## 7 EVM Bill of Materials, Assembly Drawing, and Schematic

### 7.1 ADS7864M Evaluation Module Bill of Materials

Table 6 contains a complete bill of materials for the ADS7864MEVM.

**Table 6. Bill of Materials**

Designators	Description	Manufacturer	Mfg. Part Number
C2 C3 C7 C10–C12 C18 C37–C39 C41 C45 C46 C48	0.1uF, 0603, Ceramic, X7R, 25V, 10%	TDK Corp.	C1608X7R1E104K
C35 C36 C42–C44 C49	1nF, 0603, Ceramic, COG, 50V, 5%	TDK Corp.	C1608C0G1H102J
C5 C6 C8 C9 C13 C15	10uF, 0805, Ceramic, X5R, 16V, 10%	Taiyo Yuden	EMK212BJ106KG-T
C1 C19	33pF, 0805, Ceramic, COG, 50V, 5%	TDK Corp.	C1608C0G1H330J
C22 C24	0.01uF, 0603, Ceramic, COG, 25V, 5%	TDK Corp.	C1608C0G1E103J
C16 C14 C25–C34	100pF, 0603, Ceramic, COG, 50V, 5%	TDK Corp.	C1608C0G1H101J
C40	1uF, 0603, Ceramic, X7R, 16V, 10%	TDK Corp.	C1608X7R1C105K
D1 D2	Green LED	Chicago Miniature	CMD15-21VGC/TR8
J1 J3–J5(Bottom Side)	10 Pin, Dual Row, SMT Socket (20 Pos.)	Samtec	SSW-110-22-S-D-VS
J1 J3–J5 (Top Side)	10 Pin, Dual Row, SMT Header (20 Pos.)	Samtec	TSM-110-01-T-D-V-P
J2	3 Terminal Screw Connector	On-Shore Tech.	ED555/3DS
J6 (Bottom Side)	16 Pin, Dual Row, SMT Socket (32 Pos.)	Samtec	SSW-116-22-S-D-VS
J6 (Top Side)	16 Pin, Dual Row, SMT Header (32 Pos.)	Samtec	TSM-116-01-T-D-V-P
J7	PCB Mount BNC	Amphenol	31-5329
JP1(Bottom Side)	5 Pin, Dual Row, SMT Socket (10 Pos.)	Samtec	SSW-105-22-S-D-VS
JP1 (Top Side)	5 Pin, Dual Row, SMT Header (10 Pos.)	Samtec	TSM-105-01-T-D-V-P
FB1–FB5	0805 size Ferrite Bead	TDK Corp.	MMZ2012D121B
R1 R2 R4 R24 R25 R29	4.99k $\Omega$ , 1%, 0805, .1W Resistor	Yageo Corp.	9C08052A4991FKHFT
R5–R14 R20 R21 R31 R36	49.9 $\Omega$ , 0603, 1%, 0.1W Resistor	Yageo Corp.	RC0603FR-0749R9L
R16–R19 R22 R23	10k $\Omega$ , 0603, 5%, 0.1W Resistor	Yageo Corp.	RC0603JR-0710KL
R26 R27	2k $\Omega$ , 0805, .1W Resistor	Yageo Corp.	9C08052A2001JLHFT
R15	0 $\Omega$ , 0603, 0.1W Resistor	Yageo Corp.	RC0603JR-070RL

**Table 6. Bill of Materials (continued)**

<b>Designators</b>	<b>Description</b>	<b>Manufacturer</b>	<b>Mfg. Part Number</b>
TP1–TP3 TP8–TP20	Red Test Point Loop	Keystone	5000
AGND DGND TP12	Black Test Point Loop	Keystone	5001
TP13–TP17 TP21 TP22 TP24	SMT Test Point Loop – Shown on Silkscreen as: A0, A1, A2, RST, RD, CS, CLOCK, EOC	Keystone	5015
U1	OPA2132, SOIC	Texas Instruments	OPA2132UA
U2	OPA2340; DGK package	Texas Instruments	OPA2340EA
U4	ADS7864	Texas Instruments	ADS7864Y/250
U5	INA159; DGK package	Texas Instruments	INA159AIDGKR
U3	SN74CBT3257PW	Texas Instruments	SN74CBT3257PWR
U6	SN74AHC1G04	Texas Instruments	SN74AHC1G04DBVT
U7	SN74AHC125	Texas Instruments	SN74AHC125PW
W1–W3 W5 W8	3 Pin Header	Samtec	TSW-103-07-L-S
W6 W7	2 Pin Header	Samtec	TSW-102-07-L-S
W4	2×3 Header	Samtec	TSW-103-07-L-D
W10	3×3 Header	Samtec	TSW-103-07-L-T
C4 C17 C20 C21 C23 C47 R3 R28 R33 W9	Not Installed		



## 7.2 Assembly Drawing

Figure 3 shows the top layer of the ADS7864MEVM and provides quick access to component designator found on the PWB. Complete Gerber files are available on request.

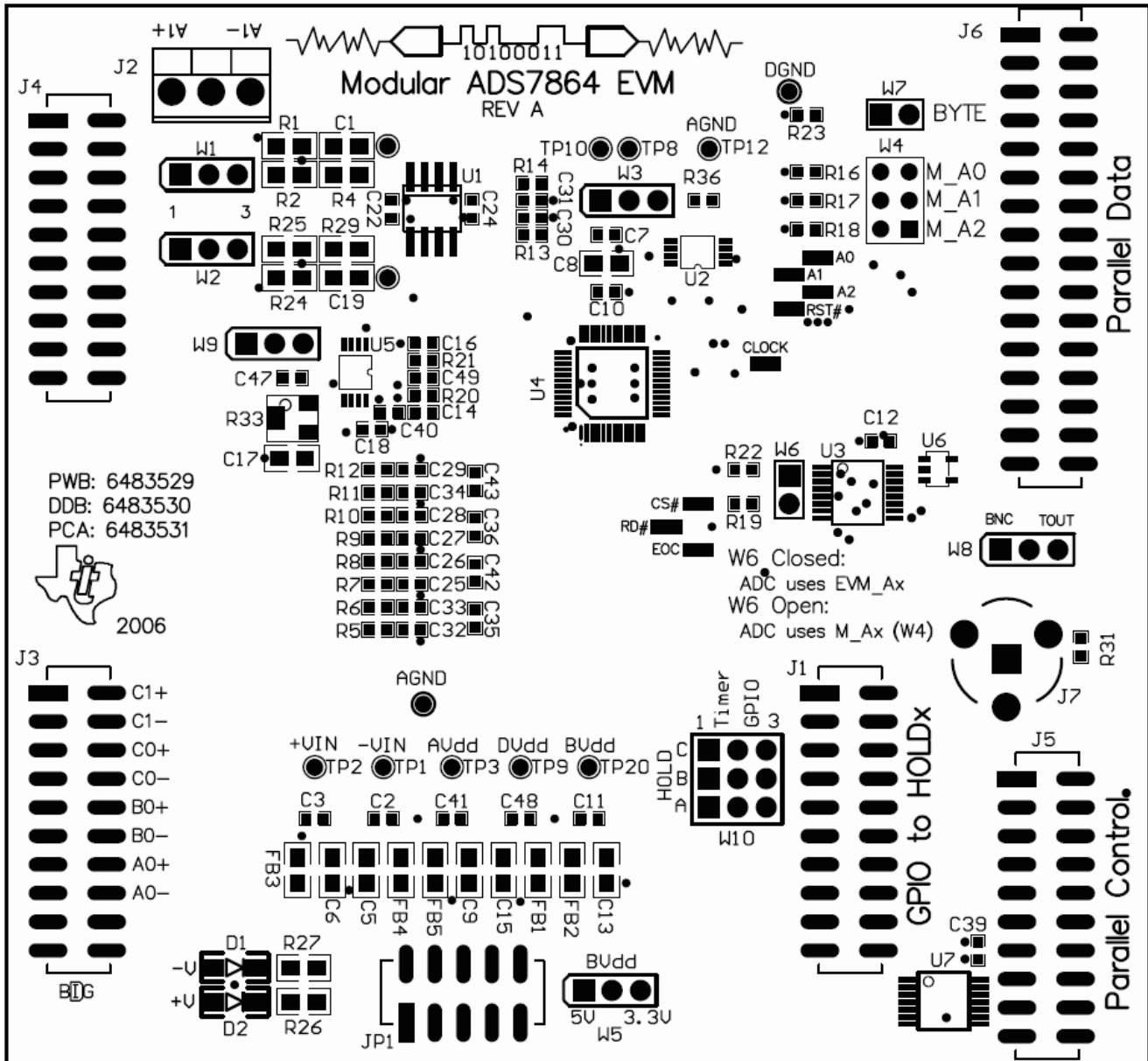


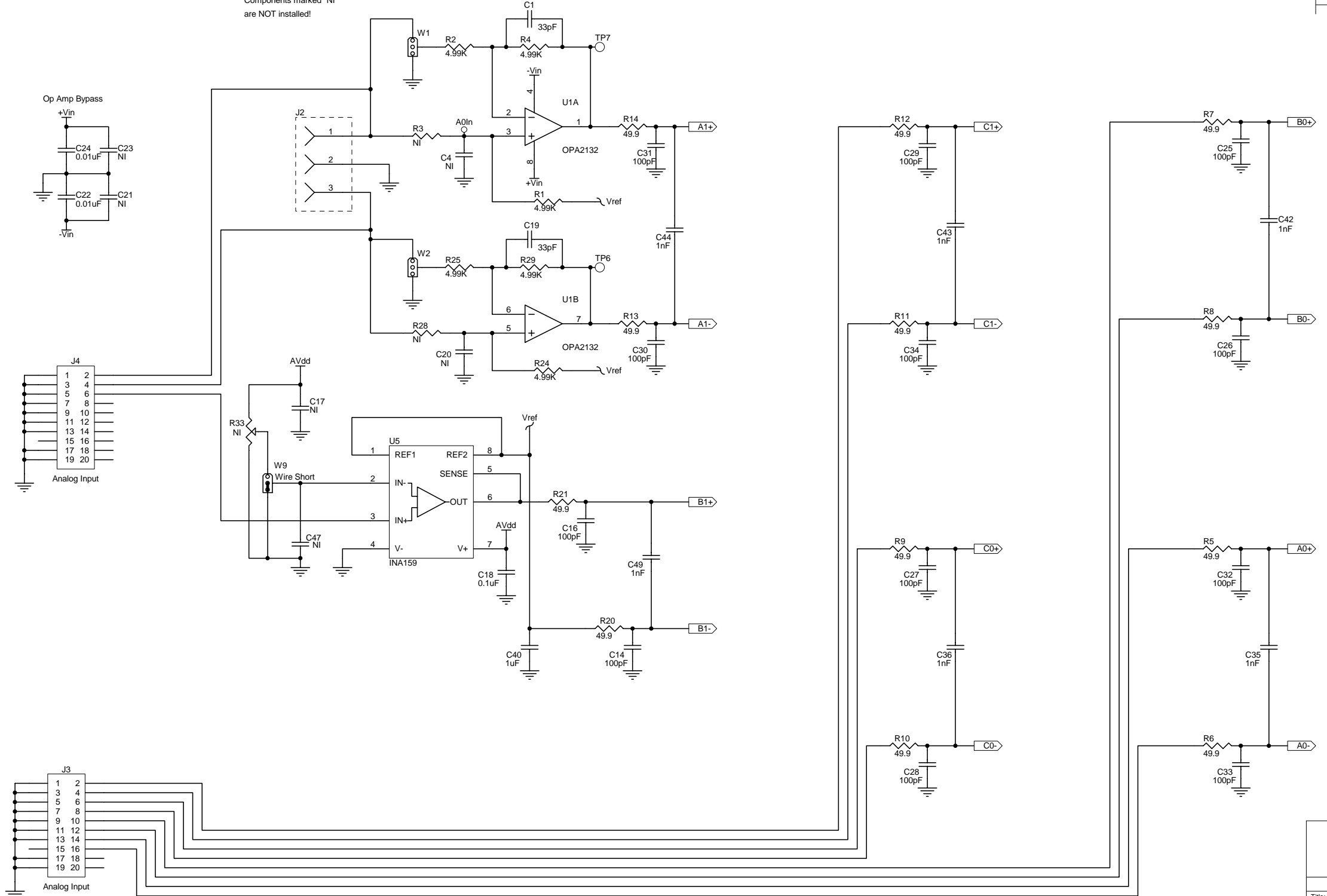
Figure 3. ADS7864MEVM Assembly Drawing

## 7.3 Circuit Schematics

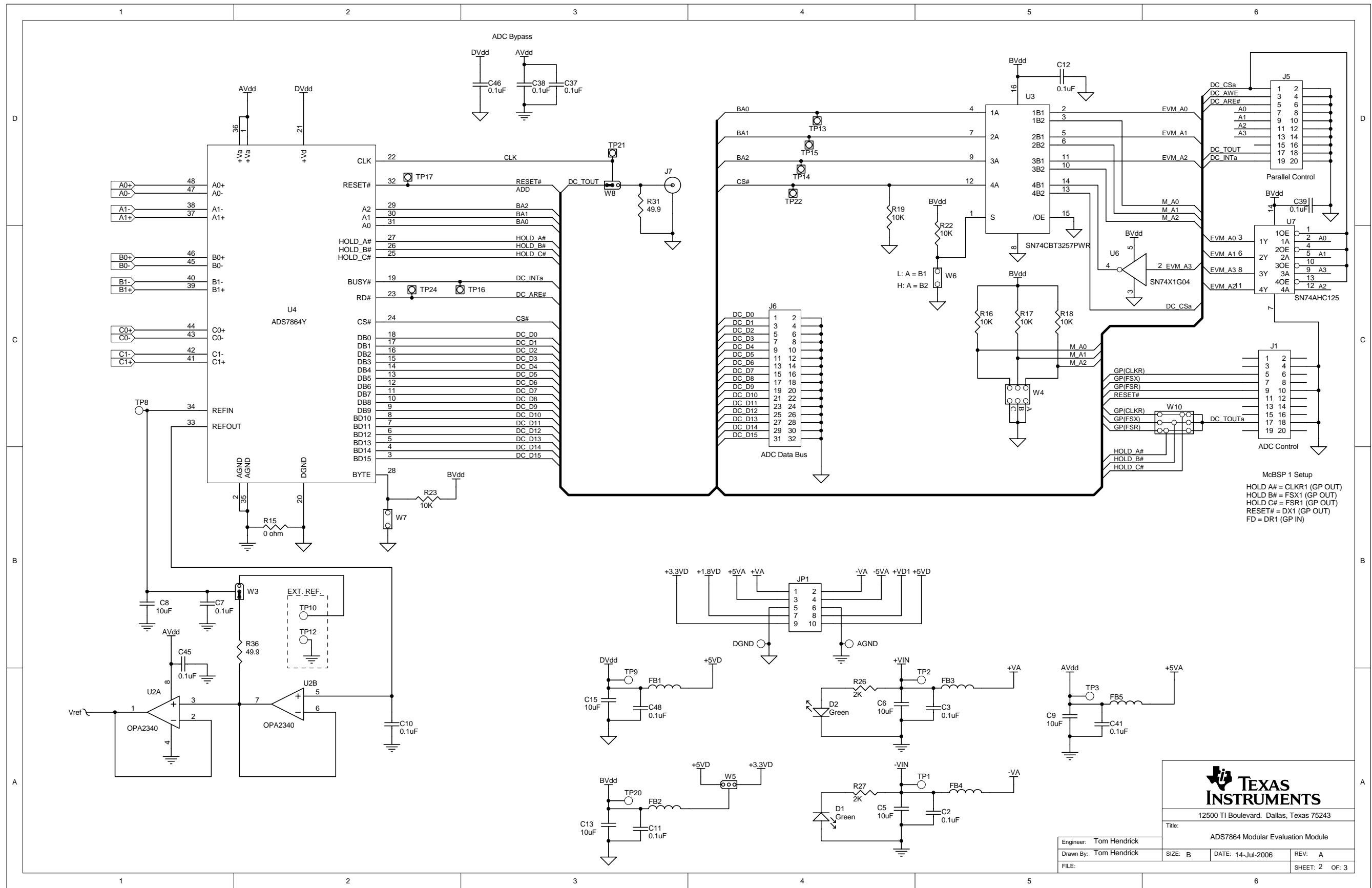
The entire circuit schematic for the ADS7864MEVM appears on the following page.

Revision History		
REV	ECN Number	Approved

Note:  
Components marked "NI"  
are NOT installed!



Title: ADS7864 Modular Evaluation Module			
Engineer: Tom Hendrick	SIZE: B	DATE: 14-Jul-2006	REV: A
Drawn By: Tom Hendrick	FILE: mADS7864_1_SH1.Sch	SHEET: 1 OF: 3	



McBSP 1 Setup  
 HOLD A# = CLKR1 (GP OUT)  
 HOLD B# = FSX1 (GP OUT)  
 HOLD C# = FSR1 (GP OUT)  
 RESET# = DX1 (GP OUT)  
 FD = DR1 (GP IN)



12500 TI Boulevard, Dallas, Texas 75243

Title:	ADS7864 Modular Evaluation Module		
Engineer:	Tom Hendrick	SIZE:	B
Drawn By:	Tom Hendrick	DATE:	14-Jul-2006
FILE:		REV:	A
		SHEET:	2 OF 3

## **8 Related Documentation From Texas Instruments**

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this document by its title and literature number. Updated documents can also be obtained through the TI Web site at [www.ti.com](http://www.ti.com)

1. *ADS7864, 500kHz, 12-Bit, 6-Channel Simultaneous Sampling Analog-to-Digital Converter* data sheet ([SBAS141](#))
2. *OPA2132, High-Speed FET-Input Operational Amplifiers* data sheet ([SBOS054](#))
3. *INA159, Precision Gain of 0.2 Level Translation Difference Amplifier* data sheet ([SBOS333](#))
4. *5-6K Interface Board User's Guide* ([SLAU104](#))
5. *DAP Signal Conditioning Board User's Guide* ([SLAU105](#))
6. *HPA-MCU Interface Board User's Guide* ([SLAU106](#))
7. *Designing Modular EVMs for Data Acquisition Products* application report ([SLAA185](#))
8. *Data Converters for Industrial Power Measurements* application report ([SBAA117](#))
9. *Op-Amps for Everyone* application report ([SLOD006](#))

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### EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of -15 V to +15 V and the output voltage range of 0 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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